

## Laboratory 5: Digital to Analog Converters (DACs)

To be performed during Week 11 (Nov. 3-7) and Week 12 (Nov. 10-14)  
Due Week 13 (Nov. 17-21)

---

### 1 Pre-Lab

This Pre-Lab should be completed before attending your regular lab section. The Lab TA will need to see your completed Pre-Lab and check it off at the start of the lab session before you can begin taking your measurements.

There are no questions to answer for this pre-lab, just read Sections 9.7, 9.8.1, and 9.8.2 in the text. In this experiment you will build and characterize two different 4-bit digital to analog converters (DACs). You will be able to observe the effects of component mismatches on the output signal levels, and we will then analyze the effect of these mismatches on the DACs ability to replicate a sinusoidal signal at its output. The first part of the lab involves building the two DACs and measuring their output characteristics. The measurement data will then be analyzed using Matlab in the second part of the lab.

### 2 Measurements

#### 2.1 Binary-Weighted Resistor DAC

Build the circuit shown in Fig. 1. Use  $\pm 10$  V power supplies for the 741 opamp. Depending on which discrete resistors are available, you may have to use multiple resistors in parallel or series to obtain the required values (e.g., use two  $2\text{ k}\Omega$  resistors in series to obtain  $4\text{ k}\Omega$ , use two  $16\text{ k}\Omega$  resistors in parallel to obtain  $8\text{ k}\Omega$ ). You do not need to include physical switches for each resistor (though you are welcome to if the stockroom has appropriate parts), you can just switch them by manually connecting them to the correct nodes. As you do this, take heart in the fact that this is likely one of the last times you will ever have to use a breadboard.

The position of each switch in Fig. 1 represents one bit of our 4-bit DAC. In the instructions that follow, we will refer to the switch configurations as the 4-bit word that represents their positions. For example,  $[S_1 S_2 S_3 S_4] = 1010$  represents switch  $S_1$  in the right position,  $S_2$  in the left position (grounded),  $S_3$  in the right position, and  $S_4$  in the left position.

1. With all of the switches in the left position (resistors grounded), measure and record the DC voltage at  $v_{out}$  using the multimeter. Instead of grounding the resistors you can also leave them open, this will have the same effect and will be easier to breadboard.

2. Now move  $S_4$  into the right position to represent the 4-bit word 0001, and measure and record the output voltage.
3. Proceed through all of the remaining 4-bit words (there are 16 in total), and measure and record the output voltage for each setting.

Double-check that your recorded values increase as the binary value of the 4-bit word increases, if they don't then you have likely made a mistake somewhere. These values will be used with Matlab in the post-processing part of this lab to gauge the performance of this DAC.

## 2.2 R-2R Ladder DAC

Build the circuit shown in Fig. 2. Again use  $\pm 10$  V power supplies for the 741 opamp. Pay careful attention to which resistors are  $1\text{ k}\Omega$  and which are  $2\text{ k}\Omega$ , this is critical for proper operation of the circuit.

Now follow the same procedure as in Section 2.1, measuring and recording the output voltage of the circuit for each of the 16 4-bit words.

## 3 Matlab Post-Processing

In this section we will gauge the performance of our DAC circuits against the ideal case. One performance measure for a DAC is how much each step varies from the size of the ideal step (**referred to as one Least Significant Bit, or LSB**). For our DAC, we have total voltage swing of  $5\text{ V}$  and 16 steps, so our LSB is  $5/16 = 0.3125\text{ V}$ . One way to quantify the DACs performance in this respect is with an Integral Non-Linearity (INL) measurement, which plots the DAC steps against the ideal case (see [http://www.maxim-ic.com/appnotes.cfm/appnote\\_number/641/](http://www.maxim-ic.com/appnotes.cfm/appnote_number/641/) for more details on this and other DAC performance metrics).

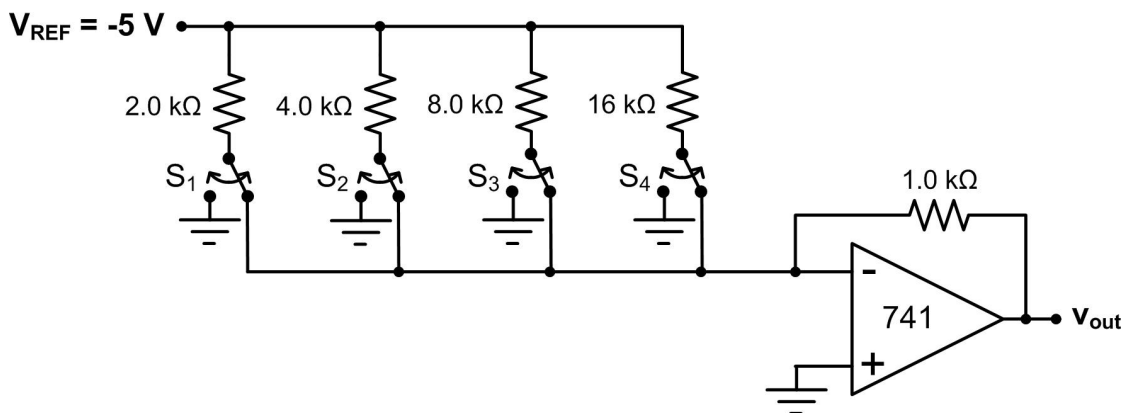


Figure 1: Binary-weighted resistor DAC schematic.

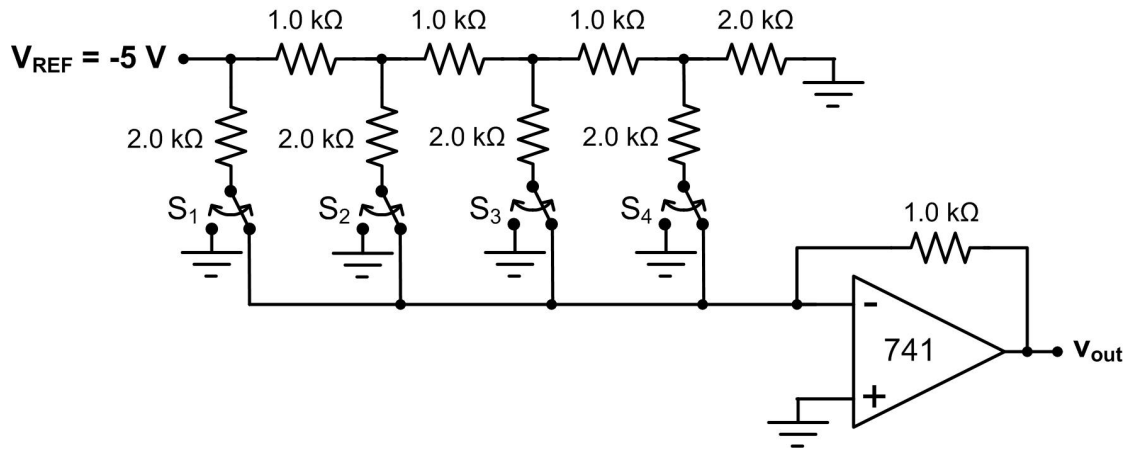


Figure 2: R-2R Ladder DAC schematic.

1. Enter your output levels for each DAC as vectors in Matlab (e.g., `Out_BW = [0.0021 0.3147 ... 4.783]`).
2. Generate a vector of the ideal DAC output levels with `Ideal = 5*[0:1:15]/16`.
3. Generate a vector for the steps with `Step = [1:1:16]`.
4. Generate a plot to compare the output characteristics for each DAC with the ideal case with `plot(Step, Out_BW, 'o', Step, Ideal)`. Add a legend, axes labels, and a title to each plot and include them in your report.
5. Generate a plot of the INL at each step with `plot(Step, (Out_BW-Ideal)/0.3125, 'o')`. Again add a legend, axes labels (the y-axis is in units of LSBs), and a title, and generate one plot for each DAC and include them in your lab report.

One of the ways DAC non-linearities will manifest themselves is in increased distortion for signals that are passed through the DAC. This can be observed by passing a sinusoidal signal through the DAC and observing the spectral (frequency domain) content of the DAC output. Ideally, the DAC would have an infinite number of output levels and the sinusoid would be perfectly replicated at the output and we would see a single tone in the frequency domain view of the output. Any real DAC will add distortion from the quantization error that is introduced, and this can be observed as harmonics of the original sinusoid that will be present in the frequency domain representation of the DAC output. These harmonics are undesirable, and the effect of the DAC non-linearities that are quantized by the INL measurement is to increase the size of these harmonics.

To observe this effect in our DACs, we will use Matlab to observe the effects of passing a sine wave through each of our DACs.

1. Download the Matlab m-file `FreqAnalysis.m` from the Laboratory section of the course website. This file takes your vector of DAC output levels as an argument, and

plots what the output of your DAC would be for a 100 Hz sinusoidal input sampled at 2 kHz.

2. Run this m-file for the Binary-Weighted DAC, supplying your vector of DAC output levels as the argument. The first plot shows one cycle of the sine wave in the time domain for three cases: the ideal case which assumes the DAC has an infinite number of output levels, the case of an ideal 4-bit DAC, and the case of your real 4-bit DAC. The second plot shows the power spectral density (the signal power in dB at each frequency) in the output for each of the three cases. Include these plots in your lab report.
3. Run this m-file for the R-2R DAC, and include these plots in your lab report.

## 4 Analysis

Answer the following questions in the analysis section of your lab report:

1. Discuss which DAC topology had better linearity, and why you would (or would not) expect this to be the case.
2. How would you expect these DACs to perform for high frequency inputs? For better high frequency components, would you want smaller or larger resistor values? Discuss the relative merits of choosing large or small resistors for the DAC.
3. One of the effects of reducing the size of the resistors is that the parasitic switch resistances could start to become significant relative to the resistors. What would the output levels be for a 3-bit Binary-Weighted Resistor DAC where the switch resistance in Fig. 9.39 of the text was  $0.25R$ ?